ASA-1003-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	C. OKAMOTO et al.
Serial No.:	10/687,753
Filed:	October 20, 2003
For:	METHOD OF MOUNTING ELECTRONIC CIRCUIT CHIP
Group:	2841
Examiner:	A. Getachew

APPEAL BRIEF

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

July 12, 2007

Sir:

This Appeal Brief is responsive to the Final Rejection mailed June 27, 2006.

In accordance with 37 CFR §41.37, the Appellants address the following items.

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I. REAL PARTY IN INTEREST

The real party in interest in this application is the assignee of record, Hitachi, Ltd.

II. RELATED APPEALS AND INTERFERENCES

There are no related prior or pending appeals, judicial proceedings or interferences known to the appellant which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 15-20 are currently pending. Claims 15 and 18 have been finally rejected and are the subject of this appeal. Claims 16, 17, 19 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and are not the subject of this appeal. Claims 1-14 have been canceled without prejudice or disclaimer.

IV. STATUS OF AMENDMENTS

All previously filed amendments have been entered. No amendments have been filed subsequent to the final rejection, although a Reply to the final rejection was filed December 27, 2006, without amendments to the claims.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention solves a need in the prior art for a foldable rectangular sheet to which an electronic circuit chip is mounted, and a method for mounting the electronic circuit chip to the foldable rectangular sheet.

The prior art has known various noncontact identification (ID) cards incorporating an electronic circuit chip mounted on a rigid substrate or card. In these prior art constructions, the card should not be folded, to avoid damage to the electronic circuit chip. Hence, the card has been constructed typically of a rigid material such as plastic, which is not easily folded or bent.

The present inventors, believing that a foldable sheet bearing the electronic circuit chip would be more convenient, set out to invent such a sheet and a method of mounting the chip to the sheet, such that the chip would not be damaged by expected folding of the sheet. To this end, the inventors have devised a foldable rectangular sheet to which an electronic circuit chip is mounted at a position which is not on any of a plurality of predetermined potential fold lines, defined in terms of the dimensions of the sheet.

More particularly, with reference to the present specification and drawing, Fig. 1 shows an electronic circuit chip 1 in which electronic circuits are integrated on a silicon chip. A capacitor 2 and an antenna 3 are connected to the electronic circuit chip 1 for reading data from the electronic circuit chip 1 in a noncontact manner. Specification at page 5, lines 7-15.

When an electromagnetic wave is applied to the above-mentioned circuit, the electromagnetic wave induces a current running through the capacitor through the antenna 3, thereby charging the capacitor 2. The power charged in the capacitor 2

causes the electronic circuit 1 to be energized so that data previously stored is transmitted in the form of an electromagnetic wave from the antenna 3. Accordingly, through the application of an electromagnetic wave, the data stored in the electronic circuit chip can be read in a noncontact manner. Specification at page 5, lines 16-27.

Fig. 2a shows a condition in which plural circuits are mounted on paper, by way of a nonlimiting example of a foldable rectangular sheet. Reference numeral 200 denotes the outer surface of a sheet on which the circuits are mounted. In the figure, reference numerals 210a to 210d denote configuration examples of the circuits which are mounted on the exemplary paper sheet. As noted in the specification at page 6, lines 6-9, the circuit 210d is illustratively bonded so as to be held between two sheets 400, 401 (201, 203) or to a rear surface of a paper sheet 500.

Further, the circuits are mounted on the paper sheet in such a configuration that the electronic circuit chips 1 are prevented from being mounted at a position on a crease which is created in the paper sheet, as indicated by dashed lines, when the paper sheet is folded. This figure shows such an example that the paper sheet is possibly folded into 1/2, 1/3 or 1/4 in the lateral direction thereof, and is possibly folded into 1/2 or 1/4 in the longitudinal direction. The dashed lines in the figure represent creases when the paper sheet is folded as mentioned above. Specification at page 6, lines 10-22.

As disclosed in the present specification, the positions where creases might possibly be created are determined in advance so that an electronic circuit chip 1 is not located thereon. By similar consideration, even if no folding configuration has

been decided, configurations which are usually used in various paper folding methods in accordance with kinds or uses of the paper sheet are utilized to determine those positions at which an electronic circuit chip will not be mounted. That is, in general, a crease may be considered to be possibly created at any of positions obtained by 1/n of the length of the paper sheet, where n is an integer, that is, in general 2, 3, 4, 5, 6, 8, 16 in both vertical and horizontal directions, or in other words, positions which are 1/2, 1/3, 1/4, 1/6, 1/8, 1/16 of the length of the paper sheet in each of the longitudinal and lateral directions. By locating the electronic circuit chip on the paper sheet at a position other than such a position where a crease may be created, it is possible to prevent the electronic circuit chip 1 from being damaged due to a large moment force exerted when the paper sheet is folded. Specification at page 6, line 23 through page 7, line 18.

Claims 15 and 18 are independent claims.

A. Summary of the Subject Matter of Independent Claim 15

Claim 15 recites a method of mounting an electronic circuit chip on a foldable rectangular sheet which has first and second sides, the second sides being not wider than the first sides. The chip is mounted, according to the method, at a position which is not on any one of a line passing through positions of one-half of the length of the first sides and being parallel with the second sides, lines passing respectively through positions of one-third or one-fourth of the length of the first sides and being parallel with the second sides, and a line passing through positions of one-half of the second sides and being parallel with the first sides. In other words, the method is performed so that the chip is <u>not</u> mounted on specified lines, as described above with reference to pages 6-7 of the specification, which is advantageous in that it

preserves those lines for predetermined folds of the sheet, or even for common folds in the case where no configuration is previously known for the sheet.

The references to the specification are to show support for the claimed subject matter, as required by 37 CFR §41.37, and are not to be considered unduly limiting of the scope of any claim, including claim 15.

D. Summary of the Subject Matter of Independent Claim 18

Claim 18 recites a foldable rectangular sheet to which an electronic circuit chip is mounted, characterized in that the electronic circuit chip is located at a position which is not on any one of a line passing through positions of one-half of the length of the first sides and being parallel with the second sides, lines passing respectively through positions of one-third or one-fourth of the length of the first sides and being parallel with the second sides, and a line passing through a position of one-half of the second sides and being parallel with the first sides. As noted above with reference to pages 6-7 of the specification, this construction is advantageous in that, by not mounting the chip on specified lines, those lines are preserved for predetermined folds of the sheet, or even for common folds in the case where no configuration is previously known for the sheet. Thus, the electronic circuit chip of claim 18 can be prevented from being damaged without reducing the expected usefulness of the sheet, simply by avoiding the mounting of the chip on the lines set forth in the claim which are typical locations for creases or folds.

Other embodiments supported by the claims are set forth in the specification, and thus the above discussion should not be deemed unduly limiting of the scope of any claim. It is believed, however, that the foregoing discussion satisfies the requirements of 37 CFR §41.37.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 15 and 18 stand finally rejected under 35 USC §102(e) as being anticipated by Blanc, et al., US 6,437,985 (Blanc).

B. Claim 18 also stands finally rejected under 35 USC §102(b) as being anticipated by Kamiyama, JP 62-25096 (Kamiyama).

C. Claim 15 also stands finally rejected under 35 USC §103(a) as being unpatentable over Kamiyama in view of Usami, et al., US 5,689,136 (Usami).

VII. ARGUMENT

References Relied Upon by the Examiner

Blanc, et al., US Patent No. 6,437,985 (Blanc)

Kamiyama, JP Patent Application Publication No. 62-25096 (Kamiyama)

Usami, et al., US Patent No. 5,689,136 (Usami)

A. Claims 15 and 18 stand finally rejected under 35 USC §102(e) as being anticipated by Blanc, et al., US 6,437,985 (Blanc).

Claim 15

Independent claim 15 recites a method of mounting an electronic circuit chip on a foldable rectangular sheet which has first and second sides, the second sides being not wider than the first sides. The chip is mounted, according to the method, at a position which is not on any one of a line passing through positions of one-half of the length of the first sides and being parallel with the second sides, lines passing respectively through positions of one-third or one-fourth of the length of the first sides and being parallel with the second sides, and a line passing through positions of one-half of the second sides and being parallel with the first sides. In other words, the method is performed so that the chip is not mounted on specified lines, which is advantageous in that it preserves those lines for predetermined folds of the sheet, or even for common folds in the case where no configuration is previously known for the sheet. See page 6, line 27 through page 7, line 3 of the present specification.

Blanc discloses, in column 5, lines 51-53, that the interface support film 1 "must be able to be folded outside the zone of the chip for example into two or four."

In the same column, at lines 56-57, Blanc teaches, "In other cases, it should be possible to crumple or crease at random, the folds having at least the radius quoted above" (less than 2.5 mm, and preferably less than 1 mm, as stated in line 55). Thus, Blanc does not limit the mounting of the chip so as to require the chip to be off the claimed lines.

The reason that Blanc does not so limit the location of the chip is supported in column 8, lines 2-6; namely, "The microcircuit is placed advantageously in a corner of the support film and directly above it. Preferably the choice is to position the chip in the corner of the label to reduce mechanical stresses linked to handling but also to have the largest possible surface free for printing." By this teaching, it appears that Blanc is concerned with "avoiding the chip", rather than "avoiding the fold" as in the present invention. At least, there is no suggestion that the fold lines themselves are of concern, particularly in light of the teaching that the sheet can be "crumpled at random."

Specifically, there seems to be no suggestion by Blanc that the chip should not be mounted on any one of the claimed lines:

> a line passing through positions of one-half of the length of the first sides and being parallel with the second sides;
>
> lines passing respectively through positions of one-third or one-fourth of the length of the first sides and being parallel with the second sides;
>
> a line passing through positions of one-half of the second sides and being parallel with the first sides.

Claim 18

Independent claim 18 is similarly distinguishable from Blanc, requiring that "the electronic circuit chip is located at a position which is not on any one of a line

passing through positions of one-half of the length of the first sides and being parallel with the second sides, lines passing respectively through positions of one-third or one-fourth of the length of the first sides and being parallel with the second sides, and a line passing through a position of one-half of the second sides and being parallel with the first sides."

B. Claim 18 also stands finally rejected under 35 USC §102(b) as being anticipated by Kamiyama, JP 62-25096 (Kamiyama).

Claim 18

Independent claim 18 is also distinguishable from Kamiyama.

Kamiyama discloses that partial regions of a card body, in a crosswise direction and in a lengthwise direction intersected with each other and formed at the substantially central portion of the card body, become bent more easily than other regions. As a result, the semiconductor device of Kamiyama is embedded at a position of the card body excluding the above regions, so as to protect the device even if the card body is bent substantially due to an external force. See page 3, lines 16-24 of the translation of Kamiyama (attachment to Reply after final rejection, filed November 27, 2006).

Kamiyama, thus, is not seen to teach or fairly suggest that the regions that are bent more easily are located on the lines as claimed. More particularly, it seems that Kamiyama is most concerned with being sure that the device is not located where the card is weakest, with such weaknesses not being defined as required by the claim, but rather at the substantially central portion of the card body one-by-one in a crosswise direction and in a lengthwise direction.

On the other hand, claim 18 recites a foldable rectangular sheet to which an electronic chip is mounted, characterized in that "the electronic circuit chip is located at a position which is not on any one of a line passing through positions of one-half of the length of the first sides and being parallel with the second sides, lines passing respectively through positions of one-third or one-fourth of the length of the first sides

and being parallel with the second sides, and a line passing through a position of one-half of the second sides and being parallel with the first sides." As noted above, this construction is advantageous in that, by not mounting the chip on specified lines, those lines are preserved for predetermined folds of the sheet, or even for common folds in the case where no configuration is previously known for the sheet. Thus, the electronic circuit chip of claim 18 can be prevented from being damaged without reducing the expected usefulness of the sheet, simply by avoiding the mounting of the chip on the lines set forth in the claim which are typical locations for creases or folds. Such limitations and advantages are neither taught nor suggested by Kamiyama.

C. Claim 15 also stands finally rejected under 35 USC §103(a) as being unpatentable over Kamiyama in view of Usami, et al., US 5,689,136 (Usami).

Claim 15

For similar reasons, independent claim 15 is patentably distinguishable from Kamiyama. As noted above, claim 15 recites a method of mounting an electronic circuit chip on a foldable rectangular sheet which has first and second sides, the second sides being not wider than the first sides. The chip is mounted, according to the method, at a position which is not on any one of a line passing through positions of one-half of the length of the first sides and being parallel with the second sides, lines passing respectively through positions of one-third or one-fourth of the length of the first sides and being parallel with the second sides, and a line passing through positions of one-half of the second sides and being parallel with the first sides. In other words, the method is performed so that the chip is not mounted on specified lines, which is advantageous in that it preserves those lines for predetermined folds of the sheet, or even for common folds in the case where no configuration is previously known for the sheet. See page 6, line 27 through page 7, line 3 of the present specification.

Kamiyama, however, while disclosing that certain partial regions of a card body become bent more easily than other regions (as discussed above), nevertheless does not teach or fairly suggest that the regions that are bent more easily are located on the lines as claimed. More particularly, it seems that Kamiyama is most concerned with being sure that the device is not located where

the card is weakest, with such weaknesses not being defined as required by the claim, but rather at the substantially central portion of the card body one-by-one in a crosswise direction and in a lengthwise direction.

Usami is applied as disclosing an electronic circuit chip 114 with another planar electronic element (coil 115) mounted to a flexible rectangular IC (integrated circuit) card 113 for the purpose of providing power to the chip 114 and transferring data to/from the chip 114. However, Usami does not teach the features missing from Kamiyama as outlined above, including mounting the chip at a position which is not on any one of a line passing through positions of one-half of the length of first sides of the IC card 113 and being parallel with second sides of the IC card, lines passing respectively through positions of one-third or one-fourth of the length of the first sides and being parallel with the second sides, and a line passing through positions of one-half of the second sides and being parallel with the first sides. Thus, without addressing the propriety of combining Usami with Kamiyama, it is sufficient to note that any combination of these two references fails to reach the limitations of claim 15.

VIII. CONCLUSION

For the foregoing reasons, the Appellants respectfully submit that the rejection of the claims on appeal should be reversed and the application allowed.

IX. FEES

A Credit Card Payment Form is enclosed, which includes the $500.00 filing fee for this Brief in support of an appeal.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, or credit any overpayment of fees, to the deposit account of Mattingly, Stanger, Malur & Brundidge, P.C., Deposit Account No. 50-1417 (referencing attorney docket no. ASA-1003-02).

Respectfully submitted,

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CLAIMS APPENDIX

1. – 14. (canceled)

15. (previously presented) A method of mounting an electronic circuit chip together with another planar electric element to a foldable rectangular sheet having first sides and second sides which are not wider than the first sides, the electronic circuit chip-mounted sheet comprising a finished product that is foldable along at least one fold line of the foldable rectangular sheet, the method being characterized in that the electronic circuit chip is mounted to the foldable rectangular sheet at a position which is not on any one of a line passing through positions of one-half of the length of the first sides and being parallel with the second sides, lines passing respectively through positions of one-third or one-fourth of the length of the first sides and being parallel with the second sides, and a line passing through positions of one-half of the second sides and being parallel with the first sides.

16. (previously presented) A method of mounting an electronic circuit chip as set forth in claim 15, characterized in that a rod-like antenna is mounted on the sheet so as to extend in a direction coincident with a direction of a crease line which is caused when said sheet is folded in a predetermined folding manner.

17. (previously presented) A method of mounting an electronic circuit chip as set forth in claim 15, characterized in that a rod-like antenna is mounted on the sheet so as to cross at least one of the lines.

18. (previously presented) A foldable rectangular sheet to which an electronic chip is mounted, the electronic circuit chip-mounted sheet comprising a finished product that is foldable along at least one fold line of the foldable rectangular sheet, the foldable rectangular sheet having first sides and second sides not wider than the first sides, characterized in that the electronic circuit chip is located at a position which is not on any one of a line passing through positions of one-half of the length of the first sides and being parallel with the second sides, lines passing respectively through positions of one-third or one-fourth of the length of the first sides and being parallel with the second sides, and a line passing through a position of one-half of the second sides and being parallel with the first sides.

19. (previously presented) A foldable rectangular sheet as set forth in claim 18, characterized in that a rod-like antenna is mounted on the sheet so as to be extended in a direction coincident with a direction of a crease line which is caused when said sheet is folded in a predetermined folding manner.

20. (previously presented) A foldable rectangular sheet as set forth in claim 18, characterized in that a rod-like antenna is mounted on the sheet so as to cross at least one of the lines.